(A) NAME OF COURSE : DIGITAL ELECTRONICS (IT401)

(B) LEVEL : FOUR

(C) BRANCH/DISCIPLINE : INFORMATION TECHNOLOGY

(D) RATIONALE :

This subject will help the students to learn facts, Concepts, principle and procedure of digital electronics. These techniques can be used for designing sequential and combinational circuits, which forms the basis of any electronic device.

(E) TEACHING AND EXAMINATION SCHEME:

Course Code	Name of Course	Teaching Scheme					Examination Scheme				Total Marks
							Theory		Practical		
		Pre-requisite	L	T	P	C	ET	PA	ET	PA	
IT-401	Digital Electronics	IT-201	3	1	2	6	75	25	50	25	175

(F) DETAILED COURSE CONTENT

CHAPTER - 1	**FUNDAMENTAL CONCEPTS** • Comparison between analog and digital signals. Different types of number system and codes used in digital computers.
CHAPTER – 2	**LOGIC GATES:** • Basic Logic Gates: Logic symbols and truth table of all gates: AND, OR, NOT, NAND, NOR, EX-OR, EX-NOR. Realization of all other gates using universal gate.

CHAPTER – 3	**BOOLEAN ALGEBRA** • Rules and laws of Boolean algebra, Demorgan's theorem. Evaluation of logic expression, algebraic reduction of Boolean expressions
CHAPTER – 4	**COMBINATIONAL LOGIC DESIGN** • Introduction to logic design • Karnaugh map representation of logical functions, Simplification of logical function using K-map, (2, 3, 4 variable) Sum of products (SOP) Pproduct of Sum (POS) . • Don't care conditions. • Design example: half adder, full adder, Half subtractor, full subtractor, BCD to seven-segment decoder (using k-map) • Gray to binary code converter (using k-map)
CHAPTER – 5	**COMBINATIONAL LOGIC DESIGN USING MSI AND LSI CIRCUITS** • Multiplexer (:1) demultiplexer (1:4), Decoder (3:8) encoder (8:3) using combinational logic design. • BCD adder, using (7483). ALU(74181). Digital comparator (7485),Parity generator/checkers(74180). • Code converters: BCD to binary(74184), Binary to BCD(74185A) • Priority encoder: Decimal to BCD(74147), Octal to binary priority encoder (74148) Hexadecimal to binary priority encoder using 74148 encoders. Decoder/drivers for display device:BCD to decimal decoder/driver (7447, 7448)
CHAPTER – 6	**LOGIC FAMILIES** • Digital integrated circuits, its introduction • Introduction: RTL, DTL, IIL, ECL, MOS families • Propagation delay time, speed, power consumption, fan_in , fan_out. • TTL and C-MOS logic families: Introduction • Analysis of open collector and tri-state logic, Input/output parameters, advantages, applications, • IC-interfacing, TTL driving CMOS, CMO driving TTL

CHAPTER – 7	**SEQUENTIAL LOGIC CIRCUIT:** • Introduction : One bit memory cell • Flip-Flop-S-R, Clocked RS, T,D, J-K, master slave , JK • Triggering of flip-flops, analysis of clocked sequential circuits, state reduction and assignment, Flip-flop excitation table, design procedures, design of counters, design with state equation . • Registers ,shift registers. Working with SISO,SIPO,PISO,PIPO shift registers . Counters : Ripple counters, synchronous and asynchronous counters, timing sequences, Ring and Johnson counter, application of counters.
CHAPTER – 8	**SEMICONDUCTOR MEMORY** • Introduction to semiconductor memory. • Memory organization and operation. • Introduction to different types of memories , ROM, EPROM, EEPROM, RAM(static and dynamic)
CHAPTER – 9	**ANALOG TO DIGITAL AND DIGITAL TO ANALOG CONVERTERS** • Introduction to Analog to Digital conversion • Principles of Digital to Analog conversions • Introduction to OP-Amp, Block diagram of OP-Amp, IC-741, Characteristics of OP-Amp, Inverting non inverting amplifier and comparator • Digital to Analog conversion using weighted registers and R-2R ladder networks • Analog to Digital conversion using Dual slop and ramp type method. • Analog to Digital conversion using successive approximation method.

(G) SPECIFICATION TABLE SHOWING DISTRIBUTION OF MARKS AND HOURS

Chapter No.	Name of Chapter	Hours	Marks			
			K	C	A	Total Mark
1.0	Fundamental Concepts	4	4	2		6
2.0	Logic Gates	6	3	3	2	8
3.0	Boolean Algebra	6	2	3	3	8
4.0	Combinational Logic Design	7	3	3	3	9
5.0	Combinational Logic Design Using MSI And LSI Circuits	8	2	3	4	9
6.0	Logic Families	7	2	3	4	9
7.0	Sequential Logic Circuit	8	3	3	3	9
8.0	Semiconductor Memory	8	2	3	3	8
9.0	Analog To Digital And Digital To Analog Converters	10	2	3	4	9
	Total	64				75

Abbreviations: **K**=Knowledge level, **C**= Comprehension Level, **A**=Application level

(H) IMPLEMENTATION STRATEGIES

The subject will be taught as per the given teaching scheme for theory as well as practical.
The identified practical sections will be conducted along with theory section.
The subject teacher will prepare & provide learning material to students.
A CBT (Computer Based Training) may be more useful to learn these topics of digital techniques.

(I) LEARNING RESOURCES SUGGESTED TO BE USED

1. Lab manuals if available
2. CAI packages
3. OHP transparencies

(J) SUGGESTED LIST OF PRACTICALS/ DEMONSTRATIONS/

Hours: 32 **Marks:25**

i) Study and Verify the truth table of logic gates (74xx series).
ii) Realization of AND, OR, NOT and Ex-OR logic gates using NAND and NOR gate
iii) Verification of Demorgan's theorem
iv) Implementation of full adder, substractor using gates

v) Study of gray to binary code convertor using gates
vi) Study to multiplexer and demultiplexers.
vii) Implementation of combination logic circuit using mux and Dmux.
viii) Study of BCD adder
ix) Study of BCD to seven segment decoder.
x) Verification of truth table of flip flop using IC's
xi) Shift registers using D flip-flop.
xii) Presetable shift right, shift left registers.
xiii) Ripple counter using J-K flip-flop.
xiv) Decode counter 7490.
xv) Synchronous counter using J-K flip-flops.
xvi) Up/down counter.
xvii) Mod N counter using J-K flip-flop
xviii) Study of 6116 RAM.
xix) Study of 2732 EPROM

(K) REFERENCE BOOKS

Author	Title	Edition	Year of Publication	Publisher & Address
Maluino & Leach	Digital principles	Latest	2000	Tata McGraw-Hill Publishing Company Ltd. New Delhi
R.P.Jain	Modern Digital Electronics	2nd Edition	2000	Tata McGraw-Hill Publishing Company Ltd. New Delhi
V.K. Puri	Digital Electronics	1st Edition	2000	Tata McGraw-Hill Publishing Company Ltd. New Delhi

(A) COURSE TITLE AND CODE : ANALOGUE & DIGITAL COMMUNICATION (IT-405)

(B) LEVEL : FOUR

(C) BRANCH/DISCIPLINE : INFORMATION TECHNOLOGY

(D) RATIONALE :

All students in information Technology need to understand the basic theory and practice of communications by electronic means. This course covers the basic theory, and introduces the techniques used in analog and digital communication systems as well as the operation of practical communication systems

(E) TEACHING AND EXAMINATION SCHEME:

Course Code	Name of Course	Teaching Scheme					Examination Scheme				Total Marks
							Theory		Practical		
		Pre-requisite	L	T	P	C	ET	PA	ET	PA	
IT405	Analogue And Digital Communication (IT405)	-	4	-	2	6	75	25	50	25	175

(F) DETAILED COURSE CONTENT

CHAPTER - 1 SIGNALS AND ITS REPRESENTATION

- Fourier Series and Transformation
  - Fourier series: circuit analysis, power and energy, frequency spectra, applications.
  - Fourier transform: derivation, convergence, operational transforms, circuit and communications applications.
  - Properties of FT, modulation, sampling. Relationship to Laplace transform. Bode plots

CHAPTER – 2 ANALOG COMMUNICATIONS

- Amplitude modulation, frequency conversion. DSB AM, SSB, VSB. Modulators and demodulators. Superhet radio.
- Frequency modulation. Narrowband and Wideband FM. Waveforms and spectra.
- Radio and TV broadcasting.

CHAPTER-3 DIGITAL COMMUNICATIONS-I

- Baseband data transmission. Line transmission. Intersymbol interference, bit error rate.
- Sampling, PCM, TDM. Protocols. Digital transmission of analog signal

CHAPTER – 4 DIGITAL COMMUNICATION-II

- Digital modulation. PCM, Eye patterns, Delta modulation, Adaptive delta modulation, SIN performance and bandwidth of delta and PCM, Modems. Optical fiber links

CHAPTER – 5 CODING

- Coding separable codes, Prefix property, Coding efficiency, Source coding, Huffman code, Error connection codes, FEC and ARQ, Hamming distance, Minimum distance, Channel coding, Block code, Cyclic code, Convolutional code

(G) SPECIFICATION TABLE SHOWING DISTRIBUTION OF MARKS AND HOURS

Chapter No.	Name of Chapter	Hours	Marks			
			K	C	A	Total Mark
10.0	Signals and its Representation	16	10	5	5	20
11.0	Analog Communications	12	8	4	4	16
12.0	Digital communication I	12	5	4	4	13
13.0	Digital communication II	10	4	3	3	10
14.0	Coding	14	8	4	4	16
	Total	64				75

Abbreviations: **K**=Knowledge level, **C**= Comprehension Level, **A**=Application level

(H) IMPLEMENTATION STRATEGIES

Students in addition to being exposed to design methodology in the lecture session, are required to apply these in a design assignments. Examples of such an assignment include: iterative design of signals to achieve appropriate temporal and spectral characteristics; design of a pulse-amplitude-modulation system to time-division-multiplex a number of disparate communication signals.

(I) LEARNING RESOURCES SUGGESTED TO BE USED

4. Lab manuals if available
5. CAI packages
6. OHP transparencies

(J) SUGGESTED LIST OF PRACTICALS/ DEMONSTRATIONS/

Hours: 32 **Marks:25**

- Study of amplitude modulation and determinations of modulation index.
- Design AM generator and its implementation
- Design of AM detector and its implementation
- Study of FM
- Design of FM generator and its implementation
- Study of waveform synthesizer
- Verification of sampling theorem
- Time division multiplexing
- Study of PCM system-

(K) REFERENCE BOOKS

S.No.	Title	Edition & Year of Publications	Author, Publisher & Address
1	Communication System	Latest	S Hykini
2	Principle of Communication	Latest	Taub Schilling Communication System B.P. Lathi
3	Introduction To Communication Systems	Latest	Stremler,F. G. Addison-Wesley Publishing Company
4.	Digital and Analog Communications Systems	Latest	Prentice-Hall Couch, Leon W. II,
5.	Communication Systems Engineering	Latest	Proakis and Salehi Prentice Hall

(A) COURSE TITLE AND CODE : MICRO-PROCESSOR PROGRAMMING (IT-501)

(B) LEVEL : FIVE

(C) BRANCH/DISCIPLINE : INFORMATION TECHNOLOGY

(D) RATIONALE :

This subject is basically designed to introduce the students with the microprocessor and microcomputers. The micro-processor 8085 architecture, working & programming is covered which aims to introduce the students with internal working of computer & helps to develop logical ability of student to prepare programs/software.

(E) TEACHING AND EXAMINATION SCHEME

Sl. No.	Course Code	Name of Course	Teaching Scheme					Examination Scheme				Total Marks
								Theory		Practical		
			Pre-requisite	L	T	P	C	ET	PA	ET	PA	
1.	IT-501	Microprocessor Programming	IT-201	4	1	2	7	100	25	25	25	175

(F) DETAILED COURSE CONTENT

CHAPTER – 1.0 ARCHITECTURE OF MICROPROCESSOR 8085

Architecture

- 8085 microprocessor architecture
- Buses
- Registers
- Flags

Preliminary Interfacing Devices

- Buffers
- Tri-state devices
- Decoders
- Encoders
- Latches

Memories & their interfacing

- Types of memories such as ROM , PROM , EPROM, EEPROM RAM (static and dynamic)
- Memory Organisation and operation
- Study of 6116, 2732 memory chip

CHAPTER – 2.0 ASSEMBLY LANGUAGE PROGRAMMING OF 8085

Classification of Instruction

- According to format,
- According to addressing modes
- According to operations**.**

Execution of an instruction.

- Timing Cycles.
- T-state.
- Op code Fetch Cycle.
- Machine Cycle.
- Memory Read/Write Cycle.
- I/O Read/Write Cycle.
- Instruction Cycle**.**

Assembly Programs Based On

- Data Transfer
- Arithmetic
- Logical
- Branching Instructions.
- Machine Central instructions.

CHAPTER – 3.0 INTERRUPTS, SERIAL I/O, STACKS AND SUBROUTINES.

Concepts of Stacks and subroutine

- PSW (Program status word)
- Concepts of stack and instructions of stacks

Subroutines.

- Concepts of subroutine.
- Unconditional and conditional call & return.

Interrupts of 8085.

- Hardware
- Software
- **Instruction related to interrupts.**

CHAPTER – 4.0 I/O DEVICES.

- **Memory mapped I/O and I/O mapped I/O**
- **Study of 8255.**
- **Study of 8155.**

CHAPTER – 5.0 APPLICATION OF MICROPROCESSOR

Interfacing of Devices

- Interfacing of ADC/DAC (0808/0809)
- Interfacing of stepper motor.

(G) SPECIFICATION TABLE SHOWING DISTRIBUTION OF MARKS AND HOURS

Chapter No.	Name of Chapter	Hours	Marks			
			K	C	A	Total Mark
15.0	Architecture of Microprocessor 8085.	15	4	6	4	18
16.0	Assembly language Programming of 8085	19	6	6	6	22
17.0	Interrupts, Serial I/O, Stacks And Subroutines.	17	6	6	4	22
18.0	I/O Devices.	15	4	8	4	20
19.0	Application Of Microprocessor	14	6	8	6	18
Total:		80				100

Abbreviations: K=Knowledge level, **C**= Comprehension Level, **A**=Application level

(H) IMPLEMENTATION STRATEGIES :

The subject will be taught as per the given teaching scheme for theory as well as practical.
The identified practical sections will be conducted along with theory section.
The subject teacher will prepare & provide learning material to students.
CBT (Computer Based Training) may be used if available

(I) LEARNING RESOURCES SUGGESTED TO BE USED (if available)

7. Lab manuals
8. CAI packages
9. OHP transparencies

(J) SUGGESTED LIST OF PRACTICALS/ DEMONSTRATIONS

Hours:32 Marks:25

Atleast two Assembly Programs Based On:

- Data Transfer
- Arithmetic
- Logical
- Branching Instructions
- Rotate.
- Program for 8 Bit Multiplication
- Program for Finding Largest.
- Program for Sorting
- Program for Block Transfer.
- Program based on Stack.
- Program based on Subroutines.
- Program for Delay Routines.
- Initialization of 8255 in Simple I/O mode.
- A program to generate Square wave.
- Interfacing of ADC/DAC.
- Interfacing of stepper motor.

(K) REFERENCE BOOKS:

Author	Title	Edition	Year of Publication	Publisher & Address
R.P.Jain	Modern Digital Electronics			Tata Mc Graw Hill
Malvino Leach	Digital Principles.			Tata Mc Graw Hill
R.Gaonkar	8085/8080 Architecture			Penram International
A.P.Mathur	**Introduction to Microprocessor**			
B.Ram	Introduction to Microprocessor			

(A) COURSE TITLE AND CODE : PARALLEL PROGRAMME DESIGN (IT-504)

(B) LEVEL : FIVE

(C) BRANCH/DISCIPLINE : INFORMATION TECHNOLOGY

(D) RATIONALE :

Today parallel computing has emerged as a subject of enormous interest. There is a general consensus among professionals that the next generation of computers will work in parallel. It is thus essential for all students of computing and users of computers to have an understanding of the basic issues involved in parallel computing. This subject gives concepts of parallel computing, beginning from the notion of parallelism in formulating algorithms and ending with some recent work in parallel computing. After going through this course the students will have an understanding of the structure of parallel computers and their applications in various situations.

(D) TEACHING AND EXAMINATION SCHEME:

Course Code	Name of Course	Teaching Scheme					Examination Scheme				Total Marks
							Theory		Practical		
		Pre-requisite	L	T	P	C	ET	PA	ET	PA	
IT504	Parallel Program Design	IT502	3	1	-	4	75	25	-	-	100

(E) DETAILED COURSE CONTENT

CHAPTER - 1 PARALLEL COMPUTERS AND COMPUTATION

- Parallelism and Computing
  - Trends in Applications
  - Trends in Computer Design
  - 3 Trends in Networking
- A Parallel Machine Model
  - The Multicomputer
  - Other Machine Models
- A Parallel Programming Model
  - Tasks and Channels
  - Other Programming Models
- Parallel Algorithm Examples
  - Finite Differences
  - Pair wise Interactions
  - Search

CHAPTER – 2 DESIGNING PARALLEL ALGORITHMS

- Methodical Design
- Partitioning
  - Domain Decomposition
  - Functional Decomposition
  - Partitioning Design Checklist
- Communication
  - Local Communication
  - Global Communication
  - Unstructured and Dynamic Communication
  - Asynchronous Communication
  - Communication Design Checklist
- Increasing Granularity
- Preserving Flexibility
- Reducing Software Engineering Costs
- Agglomeration Design Checklist
- Load-Balancing Algorithms
  - Recursive Bisection.
  - Local Algorithms.
  - Probabilistic Methods.
  - Cyclic Mappings.
- Task-Scheduling Algorithms

- Hierarchical Manager/Worker.
- Decentralized Schemes.
- Termination Detection.

- Mapping Design Checklist
- Case Study: Floorplan Optimization
- Floorplan Algorithm Design
  - Partition.
  - Communication.
  - Agglomeration.
  - Mapping.

CHAPTER – 3 A QUANTITATIVE BASIS FOR DESIGN

- Defining Performance
- Approaches to Performance Modeling
- Developing Models
  - Execution Time
  - Efficiency and Speedup
- Scalability Analysis
- Experimental Studies
  - Experimental Design
  - Obtaining and Validating Experimental Data
  - Fitting Data to Models
- Case Study: Shortest-Path Algorithms
- Dijkstra's Algorihm.

CHAPTER -4 INTEGRATION OF COMPONENTS

- Modular Design Review
  - Provide simple interfaces.
  - Ensuring hiding of information.
  - Use appropriate tools.
  - Design checklist.
- Modularity and Parallel Computing
  - Data Distribution
  - Sequential Composition
  - Parallel Composition
  - Concurrent Composition
  - Design Rules
- Performance Analysis
- Case Study: Matrix Multiplication
  - Parallel Matrix-Matrix Multiplication

CHAPTER – 5 TOOLS

Compositional C++

- C++ Review
  - Strong Typing and Memory Management
  - Classes
  - Inheritance
- Concurrency
- Locality
  - Processor Objects
  - Global Pointers
  - Thread Placement
- Communication
  - Remote Operations
  - Synchronization
  - Mutual Exclusion
  - Data Transfer Functions
- Asynchronous Communication
- Determinism
- Mapping
  - Processor Object Placement
  - Mapping Threads to Processor Objects

CHAPTER – 6 MESSAGE PASSING INTERFACE

- The MPI Programming Model
- MPI Basics
  - Language Bindings
  - C Language Binding.
  - Fortran Language Binding.
  - Determinism
- Global Operations
  - Barrier
  - Data Movement
  - Reduction Operations
- Asynchronous Communication
- Modularity
  - Creating Communicators
  - Partitioning Processes
  - Communicating between Groups
- Other MPI Features
  - Derived Datatypes
- Performance Issues

(F) SPECIFICATION TABLE SHOWING DISTRIBUTION OF MARKS AND OURS

Chapter No.	Name of Chapter	Hours	Marks			
			K	C	A	Total Mark
20.0	Parallel Computers And Computation	10	6	8	2	12
21.0	Designing Parallel Algorithms	12	5	8	3	14
22.0	A Quantitative Basis For Design	10	6	8	4	12
23.0	Integration Of Components	10	3	6	5	12
24.0	Tools	12	6	8	8	13
25.0	Message Passing Interface	10	5	6	3	12
Total:		64				75

Abbreviations: **K**=Knowledge level, **C**= Comprehension Level, **A**=Application level

(G) IMPLEMENTATION STRATEGIES

Teachers are expected to let develop practical skills in students related to parallel computing using tools such as C++. The tutor should take the cases given at the end of various units to make students understand the concepts/idea discussed in that particular unit.

(H) LEARNING RESOURCES SUGGESTED TO BE USED(if available)

10. Lab manuals if available
11. CAI packages
12. OHP transparencies

(I) REFERENCE BOOKS

S.No.	Title	Edition, Year of Publication	Author, Publisher & Address
1.	Designing and Building Parallel Programs	2002	*By* Ian Foster Publisher: Addison Wesley Higher Education
2.	Introduction to Parallel Computing, An: Design and Analysis of Algorithms, 2/E	1998	Ananth Grama, Vipin Kumar, Anshul Gupta, George Karypis, ISBN: 0-201-64865-2 Publisher: Addison Wesley Higher Education
3.	Fundamentals of Parallel Computing	2002	by Harry F. Jordan, et al; Hardcover Publisher: Prentice Hall; ISBN: 0139011587
4.	Parallel Computing :		Quinn, Michael J., Tata Mcgraw Hill
5.	Elements Of Parallel Computing		Rajaraman V.

Note : Any book which covers the above syllabus can also be used.

(A) COURSE TITLE AND CODE : CLIENT/SERVER APPLICATION (IT-505)

(B) LEVEL : FIVE

(C) BRANCH/DISCIPLINE : INFORMATION TECHNOLOGY

(D) RATIONALE :

The aim of this subject is to make the students understand the basic concepts of client server architecture. The students will also develop competence to use structured query language to design and develop client server based application program.

1.0 TEACHING AND EXAMINATION SCHEME

Course Code	Name of Course	Teaching Scheme					Examination Scheme				Total Marks
							Theory		Practical		
		Pre-requisite	L	T	P	C	ET	PA	ET	PA	
IT- 505	Client/ Server Application	-	3	1	2	6	75	25	50	25	175

2.0 DETAILED COURSE CONTENT

CHAPTER – 1.0 AN OVERVIEW OF CLIENT SERVER ARCHITECTURE AND ORACLE

- Client server Architecture, benefit and pitfalls of client server computing, An overview of RDBMS
- Introduction to Oracle:What is Oracle server, its components, SQL, Forms, Reports, Oracle Architecture, Developer 2000 and Designer 2000
- Overview of the Data Integrity with DBMS, data concurrency: Data locks, Data security: Granting access, Extending and restricting privileges
- Data entry using form applications, Query tools and reporting application, GUIs

CHAPTER – 2 INTERACTIVE SQL

- Invoking SQL * Plus, DDL DML, DQL, The Oracle Data Types, Creating Tables, Insertion of Data into Table, Updating the contents of a Table, Deletion Operations, Modifying, Removing, Deleting, Dropping Tables, Applying Data Constraints, Query, Oracle Functions, Grouping Data from Tables in SQL, aggregate function of oracle, Numerical string and date functions in SQL, Joins: equi Join, non-equi Join, inner, outer joins.
- Sub-queries: using Unions, Intersect and Minus clause Indexes, Views Sequences.

CHAPTER – 3 PL/SQL

- PL-SQL execution environment, PL/SQL Character Set, Operators, Variables, Common Data Types, Components, PL/SQL syntax, Block structure, conditional and looping statements, Oracle transactions, Locks, error handling.

CHAPTER – 4 STORED PROCEDURES AND FUNCTIONS

- Procedures: advantages of procedures, declarative part, Executable part, Exception handling part creating procedure, Executing Procedures.
- Functions: Advantages of functions, creating, executing, Deleting a stored function.

CHAPTER – 5 DATABASE TRIGGERS

- Introduction, use of database triggers type of triggers, syntax for creating a trigger, enabling, disabling, replacing and dropping triggers, Creating Application using Database Triggers.

(G) SPECIFICATION TABLE SHOWING DISTRIBUTION OF MARKS AND HOURS

Chapter No.	Name of Chapter	Hours	Marks			
			K	C	A	Total Mark
26.0	An Overview Of Client Server Architecture And Oracle	12	2	4	4	10
27.0	Interactive SQL	14	2	6	6	14
28.0	Pl/SQL	10	2	7	6	15
29.0	Stored Procedures And Functions	12	2	6	10	18
30.0	Database Triggers	16	2	6	10	18
	Total	64	10	29	36	75

Abbreviations: **K**=Knowledge level, **C**= Comprehension Level, **A**=Application level

(H) IMPLEMENTATION STRATEGIES

Concepts of DBMS will be implemented by using Oracle 8.0/LATTER Version RDBMS Package. The teachers may make the students to develop as much as client server application programs as possible.

(I) LEARNING RESOURCES SUGGESTED TO BE USED

13. Lab manuals if available
14. CAI packages if available
15. Existing software systems for demonstrations

(J) SUGGESTED LIST OF EXPERIMENTS/ TUTORIALS:

Hours: 32 Marks :50

- List of Practical
- Assignments and Practice in developing client server programs using Oracle.
- Tutorial on selected topic may also be given.

(K) REFERENCE BOOKS

S.No.	Title	Edition, Year of Publication	Author, Publisher & Address
1.	Introduction to Database Management System	Latest	Navin Prakash Tata Mcgraw Hill
2.	Mastering Oracle 7.0 and Client/Server Computing	Latest	Steven M, Bobrowski, BPB Publications
3.	Oracle 7.0	Latest	Evan Barose BPB Publication.
4.	Oracle- the complete reference	Latest	George Koch & Kevin Loney, Oracle Press (TMH)
5.	Using Oracle 8.		William Page Jr. And Nathen Hughes Abraham silberschaty Practice Hall of India

(A) COURSE TITLE AND CODE : MINI PROJECT (IT-510)

(B) LEVEL : FIVE

(C) BRANCH/DISCIPLINE : INFORMATION TECHNOLOGY

(D) RATIONALE :

The mini-project will enable the students to integrate the knowledge and software development skills acquired during past years of diploma programme. He would be able to design and develop an identified software system independently in particular using the software taught in fifth level.

(A) TEACHING AND EXAMINATION SCHEME:

Course Code	Name of Course	Teaching Scheme					Examination Scheme				Total Marks
							Theory		Practical		
		Pre-requisite	L	T	P	C	ET	PA	ET	PA	
IT507	Mini Project	IT-407 or 502 or 505 or 506	1	-	3	4	-	-	50	25	75

(F) PROJECT DEVELOPMENT APPROACH

Project Selection

- Project must be based on the knowledge acquired by the students. Students must be aware of the languages, packages and hardware that he is using for his project.
- Repetition of projects may be avoided as far as possible.
- The students should be given some time for project selection. At the end of it, the student must submit a 3 to 4 page document giving outline of project and feasibility study report.
- Feasibility study includes:
- Time feasibility.
- Software, Hardware availability.
- Information source etc.
- The students has to independently carry out the project.
- Project may be an application software development

Project Design

In this phase the students will actually start analyzing the system and collect data/information for their project. The student should.

- The student should analyse and design the system.
- The student must adopt standard norms and procedures.
- Design must be modular & there must be clear.
- The student must submit "Synopsis" giving details about system analysis and design aspects. He should individually contact the concern teacher to clear his views about the project.

Project Development

Remaining time may be utilized for actual coding, testing, of project.

- Independent module development is necessary.
- The project guide must continuously assess their project during its development.
- Taking into consideration shortcoming & suggestions given during testing, the final software should be developed and submitted by the end of the term.

Project Report

The following section should be considered while writing the project:

- Project Title
- Feasibility study
- Design Aspect
- Developmental Aspect (including source code)
- Books/Manual referred

Project Valuation

Marks Distribution:-

- Innovative idea 5%
- Project Design 25%
- Working Model 45%
- Oral 25%

(G) IMPLEMENTATION

The teachers are expected to motivate the students to take innovative projects either from the polytechnic system or from the industry. Teachers should evaluate the project as per the guidelines given above.